

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. .... 09/652,550  
 Priority Filing Date ..... August 31, 2000  
 Inventor ..... Keiji Jono et al.  
 Assignee ..... Micron Technology, Inc. and KMT Semiconductor, LTD  
 Priority Group Art Unit ..... 2811  
 Priority Examiner ..... T. Tran  
 Attorney's Docket No. .... KM1-003  
 Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods  
 of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods  
 of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated  
 Transistor, Trench Isolation Structures Formed in a Semiconductor,  
 Memory Cells and DRAMS

*Handwritten:*  
 #4/A  
 4-29-02

**PRELIMINARY AMENDMENT**

To: Assistant Commissioner for Patents  
 Washington, D.C. 20231

From: Frederick M. Fliegel, Ph.D.  
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Sir:

This is a preliminary amendment accompanying a Request for  
 Divisional Application for the above-entitled patent application. Prior to  
 examining the application, please enter the following amendments.

**AMENDMENTS**

10007300-110801